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# Impact of Section 7

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2 **Abstract**

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This document describes the impact that the updated section 7 on  
"Hierarchical Structures" has on the other parts of the Verilog-AMS  
Language Reference Manual.

5 **Version**

**1**

6 **Date**

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# 1 Impact

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## 1.1 Overview of Changes

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Two additions have been made to section 7 to get the text in line with the IEEE 1364-2005 standard for digital Verilog:

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- Support for generate constructs;
- Support for multiple analog blocks.

36  
37

The impact is related only to the areas where these changes also need to be addressed in the other sections.

38

### 1.1.1 Section 1

39

No impact.

40

### 1.1.2 Section 2

41

No impact.

42

### 1.1.3 Section 3

43  
44  
45

In section 3.3 on Genvars the use of genvars for generate constructs should be mentioned. The LRM 2.2 text implies only use in for-loop statements.

46

### 1.1.4 Section 4

47

No impact.

48

### 1.1.5 Section 5

49

No impact.

50

### 1.1.6 Section 6

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52  
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54

In section 6.1 the analog construct is described, but with a limit of one analog block per module. The text should be updated to allow multiple analog blocks with the behavior as explained in the new section 7.

55  
56  
57  
58

Alternatively, the text currently in section 7.1 for multiple analog blocks should appear in section 6.1, while section 7.1 can suffice by stating that multiple analog blocks can appear in the body of an analog module.

59

### 1.1.7 Section 8

60

No impact.

61

### 1.1.8 Section 9

62

No impact.

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3           **1.1.9 Section 10**

4           No impact.

5           **1.1.10 Section 11**

6           No impact.

7           **1.1.11 Section 12**

8           No impact.

9           **1.1.12 Section 13**

0           No impact.

1           **1.1.13 Annex A**

2           The generate construct itself is described in the IEEE 1364-2005  
3           syntax, so below are the changes to that syntax to support analog  
4           constructs inside a generate construct. The added text is marked in  
5           blue – the section titles refer to the syntax boxes in the updated  
6           section 7.

7           **1.1.13.1 Syntax 7-1**

8           module\_keyword ::= module | macromodule | [connectmodule](#)

9           **1.1.13.2 Syntax 7-2**

0           module\_or\_generate\_item ::=  
1           { attribute\_instance } module\_or\_generate\_item\_declaration  
2           | { attribute\_instance } local\_parameter\_declaration ;  
3           | { attribute\_instance } parameter\_override  
4           | { attribute\_instance } continuous\_assign  
5           | { attribute\_instance } gate\_instantiation  
6           | { attribute\_instance } udp\_instantiation  
7           | { attribute\_instance } module\_instantiation  
8           | { attribute\_instance } initial\_construct  
9           | { attribute\_instance } always\_construct  
0           | { [attribute\\_instance](#) } [analog\\_construct](#)  
1           | { attribute\_instance } loop\_generate\_construct  
2           | { attribute\_instance } conditional\_generate\_construct

3           module\_or\_generate\_item\_declaration ::=  
4           net\_declaration  
5           | reg\_declaration  
6           | [branch\\_declaration](#)  
7           | integer\_declaration  
8           | real\_declaration  
9           | time\_declaration  
0           | realtime\_declaration  
1           | event\_declaration  
2           | genvar\_declaration  
3           | task\_declaration  
4           | function\_declaration  
5           | [analog\\_function\\_declaration](#)

6           non\_port\_module\_item ::=  
7           module\_or\_generate\_item

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```
108 | generate_region
109 | specify_block
110 | { attribute_instance } parameter_declaration ;
111 | { attribute_instance } specparam_declaration
112 | aliasparam\_declaration
```

### 1.1.13.3 Syntax 7-3

```
113 module_instantiation ::=
114     module_or_paramset_identifier [ parameter_value_assignment ]
115     module_instance { , module_instance } ;
116
117 named_parameter_assignment ::=
118     .parameter_identifier ( [ mintypmax_expression ] )
119     | .system\_parameter\_identifier ( [ constant_expression ] )
```

### 1.1.13.4 Syntax 7-9

```
120 module_or_generate_item ::=
121     { attribute_instance } module_or_generate_item_declaration
122     | { attribute_instance } local_parameter_declaration ;
123     | { attribute_instance } parameter_override
124     | { attribute_instance } continuous_assign
125     | { attribute_instance } gate_instantiation
126     | { attribute_instance } udp_instantiation
127     | { attribute_instance } module_instantiation
128     | { attribute_instance } initial_construct
129     | { attribute_instance } always_construct
130     | { attribute_instance } analog\_construct
131     | { attribute_instance } loop_generate_construct
132     | { attribute_instance } conditional_generate_construct
133
```

### 1.1.13.5 Syntax 7-10

```
134 analog\_loop\_generate\_statement ::=
135     for ( genvar\_initialization ; genvar\_expression ; genvar\_iteration )
136     analog\_statement
137
```

### 1.1.14 Annex B

138 The keyword “endgenerate” needs to be added to the list.

### 1.1.15 Annex C

139 In section C.7 the generate construct and the support for multiple  
140 analog blocks will be available from the analog-only subset as well.

### 1.1.16 Annex D

141 No impact.

### 1.1.17 Annex E

142 No impact.

### 1.1.18 Annex F

143 No impact.